1 Overview

1.1 Project

Project Name	AT32F407VGT7_WorkBench
Generated with	AT32 WorkBench V1.0.3
Date	2024-01-10

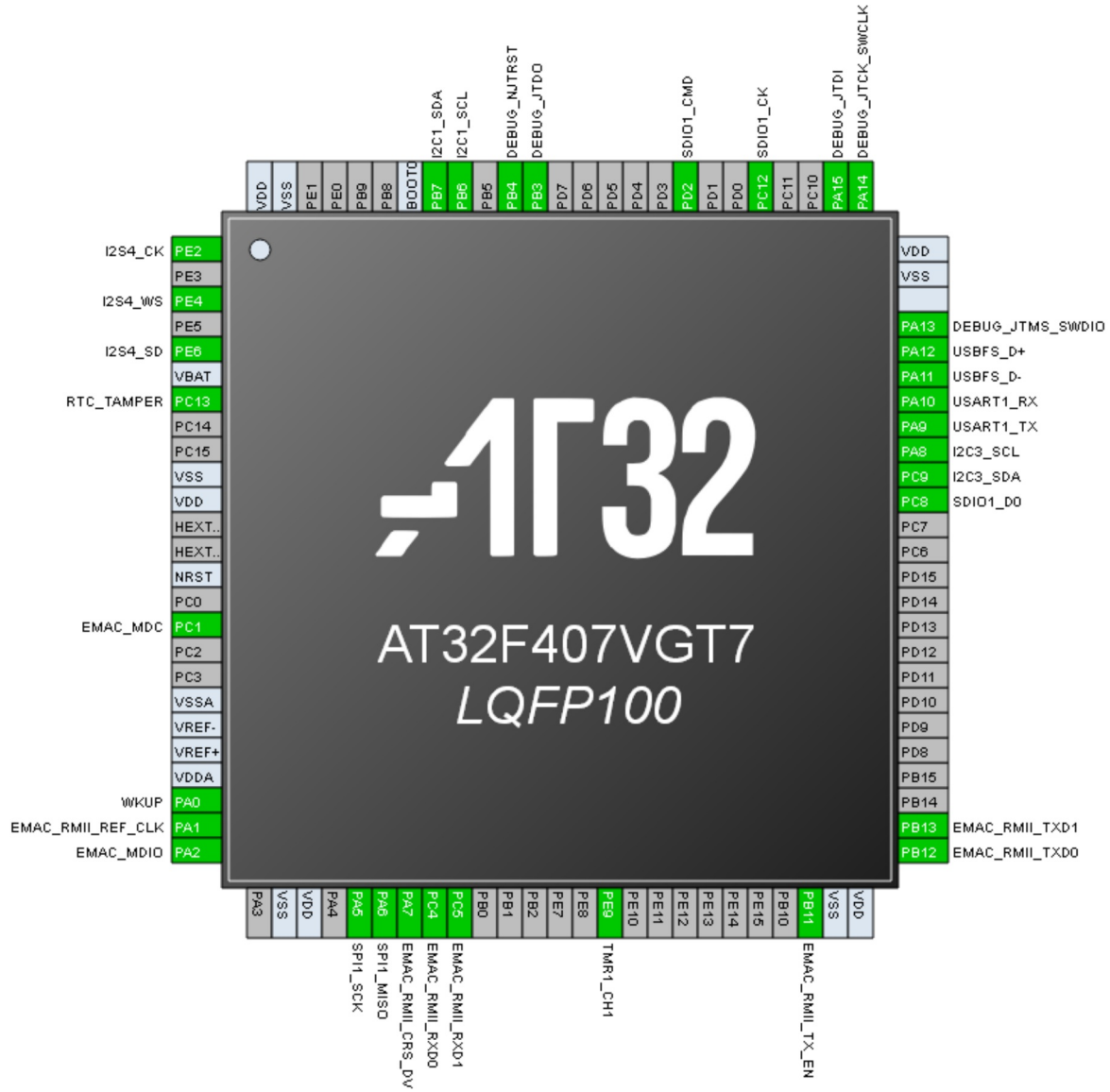
1.2 MCU Information

MCU Series	AT32F407
MCU Name	AT32F407VGT7
MCU Package	LQFP100
MCU Pin number	100
Flash	1024KB
SRAM	Default: 96KB Max: 224KB

1.3 Cores Information

Cores	ARM Cortex-M4

2 Pinout Configuration



3 Pins Configuration

Pin Number	Pin Name	Pin Type	GPIO Structure	Signal Name	Label
1	PE2	I/O	FT	I2S4_CK	
3	PE4	I/O	FT	I2S4_WS	
5	PE6	I/O	FT	I2S4_SD	
6	VBAT	S	-	-	
7	PC13	I/O	TC	RTC_TAMPER	
10	VSS	S	-	-	
11	VDD	S	-	-	
14	NRST	I/O	-	-	
16	PC1	I/O	FTa	EMAC_MDC	
19	VSSA	S	-	-	
20	VREF-	S	-	-	
21	VREF+	S	-	-	
22	VDDA	S	-	-	
23	PA0	I/O	TC	WKUP	
24	PA1	I/O	FTa	EMAC_RMII_REF_CLK	
25	PA2	I/O	FTa	EMAC_MDIO	
27	VSS	S	-	-	
28	VDD	S	-	-	
30	PA5	I/O	FTa	SPI1_SCK	
31	PA6	I/O	FTa	SPI1_MISO	
32	PA7	I/O	FTa	EMAC_RMII_CRS_DV	
33	PC4	I/O	FTa	EMAC_RMII_RXD0	
34	PC5	I/O	FTa	EMAC_RMII_RXD1	
40	PE9	I/O	FT	TMR1_CH1	
48	PB11	I/O	FT	EMAC_RMII_TX_EN	
49	VSS	S	-	-	
50	VDD	S	-	-	
51	PB12	I/O	FT	EMAC_RMII_TXD0	
52	PB13	I/O	FT	EMAC_RMII_TXD1	
65	PC8	I/O	FT	SDIO1_D0	
66	PC9	I/O	FT	I2C3_SDA	
67	PA8	I/O	FT	I2C3_SCL	
68	PA9	I/O	FT	USART1_TX	
69	PA10	I/O	FT	USART1_RX	
70	PA11	I/O	TC	USBFS_D-	

71	PA12	I/O	TC	USBFS_D+	
72	PA13	I/O	FT	DEBUG_JTMS_SWDIO	
73		-	-	-	
74	VSS	S	-	-	
75	VDD	S	-	-	
76	PA14	I/O	FT	DEBUG_JTCK_SWCLK	
77	PA15	I/O	FT	DEBUG_JTDI	
80	PC12	I/O	FT	SDIO1_CK	
83	PD2	I/O	FT	SDIO1_CMD	
89	PB3	I/O	FT	DEBUG_JTDO	
90	PB4	I/O	FT	DEBUG_NJTRST	
92	PB6	I/O	FT	I2C1_SCL	
93	PB7	I/O	FT	I2C1_SDA	
94	BOOT0	I	-	-	
99	VSS	S	-	-	
100	VDD	S	-	-	

(1) I = input, O = output, S = supply.

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog functionalities. FTa pin is 5 V-tolerant when configured as input floating, input pull-up, or input pull-down mode.However, it cannot be 5 V-tolerant when configured as analog mode.Meanwhile, its input level should not higher than VDD + 0.3V.

(3) Function availability depends on the chosen device.

(4) If several peripherals share the same GPIO pin, to avoid conflict between these multiple functions only one peripheral should be enabled at a time through the peripheral clock enable bit(in the corresponding RCC peripheral clock enable register).

(5) PC13, PC14, and PC15 are supplied through the power switch. Since the switch only drives a limited amount of current (3mA), the use of GPIOs PC13 to PC15 in output mode is limited not to be used as a current source(e.g.to drive an LED).

(6) Main function after the first battery powered domain power-up. Later on, it depends on the contents of the battery powered registers even after reset(because these registers are not reset by the main reset).For details on how to manage these GPIOs, refer to the battery powered domain and register description sections in the AT32F407 reference manual.

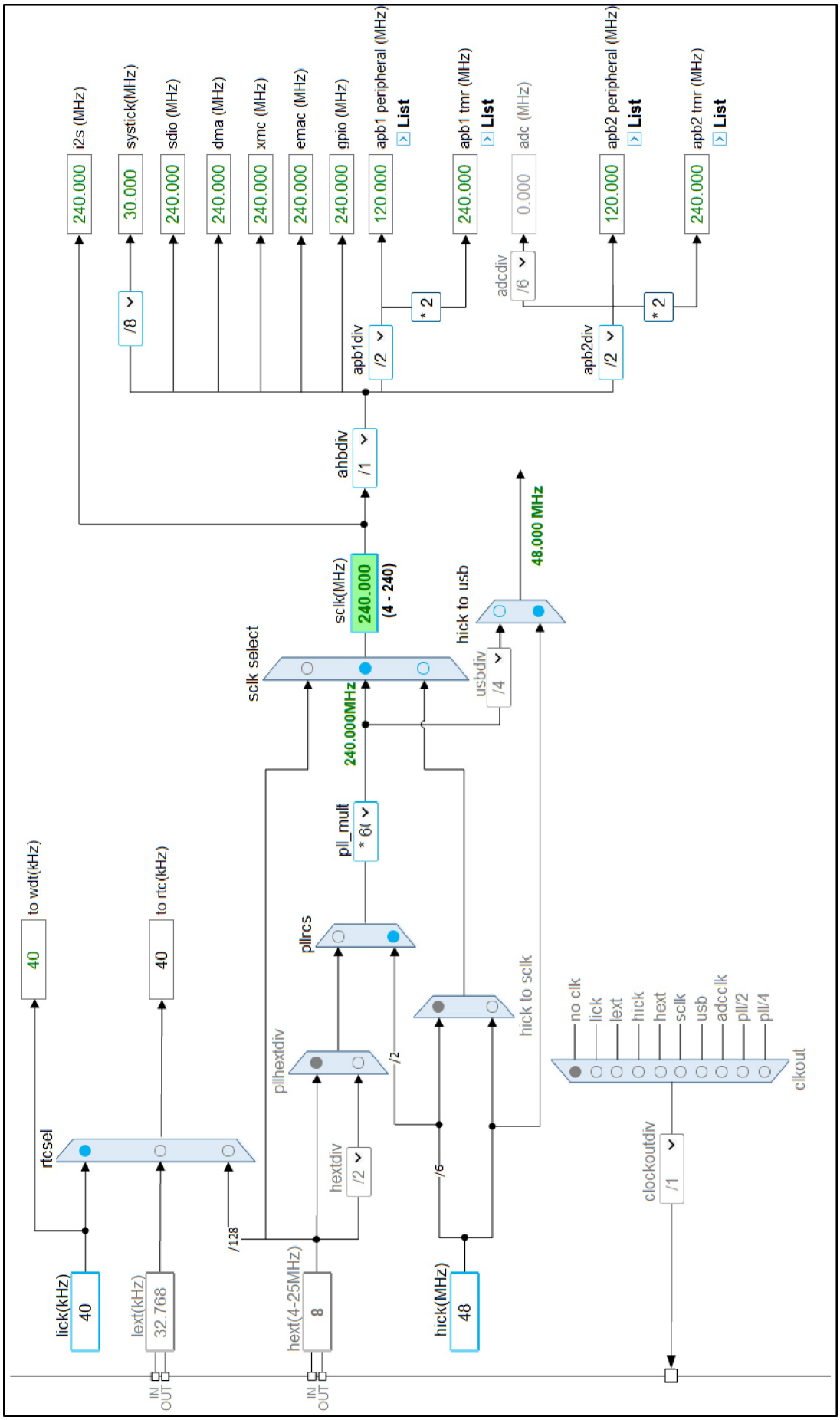
(7) This multiple function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the multi-function GPIO and debug configuration section in the AT32F407 reference manual.

(8) For the LQFP64 package, the pins number 5 and 6 are configured as HEXT_IN and HEXT_OUT after reset, the functionality of PD0 and PD1 can be remapped by software on these pins.However, for the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping.For more details, refer to multi-function GPIO and debug configuration section in the AT32F407 reference manual.

(9) SPI2, I2S2, and I2C2 are not available when the Ethernet MAC is being used.

(10) If the device boots from Flash and leaves PB2 not used, it is recommended to pull PB2 down to ground.

4 Clock Tree Configuration



5 Software Project

5.1 Project Settings

Name	Value
Project Name	AT32F407VGT7_WorkBench
Project Folder	
Toolchain/IDE	AT32_IDE
Firmware Package Name and Version	
Minimum Heap Size	0x200
Minimum Stack Size	0x400

6 Peripherals and Middlewares Configuration

6.1 ACC

Activated: Enable

6.1.1 Parameter Setting

Basic Parameters:

Compare 1(0-65535)	7980
Compare 2(0-65535)	8000
Compare 3(0-65535)	8020
Enable Trim	HICKTRIM is calibrated

6.2 DEBUG

Debug interface: JTAG (5pin)

6.3 EMAC

Mode: RMII

6.3.1 Parameter Setting

Basic Parameters:

Auto Negotiation	Disable
Speed	100Mbits/s
Duplex mode	Full duplex
Hardware Checksum	Enable
MAC address	00:00:44:45:56:01
EXINT19 WakeUp	Disable

PHY Parameters:

PHY	DM9162
PHY address(0-31)	1
Basic mode control register(0x0-0xFF)	0x0
Basic mode status register(0x0-0xFF)	0x1
Specified Configuration and Status Register(0x0-0xFF)	0x11
PHY reset bit(0x0-0xFFFF)	0x8000
Enable AUTO Negotiation bit(0x0-0xFFFF)	0x1000
Enable loopback bit(0x0-0xFFFF)	0x4000
Link status bit(0x0-0xFFFF)	0x0004
Auto-negotiation Complete bit(0x0-0xFFFF)	0x0020
PHY Duplex status(0x0-0xFFFF)	0x8000

PHY Speed status(0x0-0xFFFF)	0x4000

6.4 I2C1

I2C: I2C

6.4.1 Parameter Setting

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)(1-100000)	100000

Slave Features:

Clock Stretch Mode	Enable
Address mode	7-bit
Dual Address mode	Disable
Own address 1(0x0-0x7F)	0x0
General Call address detection	Disable

6.5 I2C3

I2C: I2C

6.5.1 Parameter Setting

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)(1-100000)	100000

Slave Features:

Clock Stretch Mode	Enable
Address mode	7-bit
Dual Address mode	Disable
Own address 1(0x0-0x7F)	0x0
General Call address detection	Disable

6.6 I2S4

Mode: Half-Duplex Transmit Only Master

6.6.1 Parameter Setting

Generic Parameters:

Operation Mode	Mode Master Transmit
Audio Protocol	I2S Philips
Data Bit Num and Channel Bit Num	16-bit Data Packed in 16-bit Channel Frame

Clock Parameters:

Selected Audio Frequency	8 KHz
Real Audio Frequency	
Error between Selected and Real	
Clock Polarity	Low

6.7 PWC

Power voltage monitoring enable: Enable
Standby wake-up pin 1 enable: Enable

6.7.1 Parameter Setting

Basic Parameters:

Power voltage monitoring enable	Enable
Power voltage monitoring boundary select	Unused
Interrupt/EveJnt	Interrupt
Trigger Polarity	Rising Edge

6.8 RTC

Activate Clock Source: Enable
Activate Calendar: Enable
Tamper Enable: Enable

6.8.1 Parameter Setting

General:

Predivider value(0-1048575)	32767

Calendar Time:

Hours(0-23)	0
Minutes(0-59)	0
Seconds(0-59)	0

Calendar Date:

Year(1970-2099)	2023
Month	January
Date(1-31)	1

Tamper:

Tamper Trigger Edge	Low Level
Interrupt	Disable

6.9 SDIO1

Mode: SD Card 1bit bus width

6.9.1 Parameter Setting

Basic Parameters:

Clock division(0-1023)	0
SDIO_CK edge selection	SDIO_CK generated on the rising edge
Power saving mode enable	Disable
Hardware flow control enable	Disable
Clock divider bypass	Disable

6.10 SPI1

Mode: Half-Duplex Slave Receive

6.10.1 Parameter Setting

Basic Parameters:

Interface protocol	Motorola
Frame bit num	8 Bits
First Bit	MSB First

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disable
CS Signal Type	Software

6.11 TMR1

Activated: Enable
Channel1 mode: Output_CH1

6.11.1 Parameter Setting

Counter Settings:

Divider value (16 bits value)(0-65535)	0
Counter Direction	Up
Period Value (16 bits value)(0-65535)	65535
Clock divider	No Divider
Repetition of period value (8 bits value)(0-255)	0
Period buffer enable	Disable
Overflow Event	From counter/ovfswtr/sub-timer

Primary mode settings:

Synchronize with sub-timer	Disable
Primary TMR output selection	Reset

Break and Dead-time settings:

Break State	Disable
Brake Input Validity	Low
Automatic Output State	Disable
Frozen channel status when holistic output enable	Disable
Frozen channel status when holistic output disable	Disable
Write Protected Configuration	Off

Output Channel 1:

Mode	Disconnected
Channel data (16 bits value)(0-65535)	0
Channel output buffer	Disable
CH Polarity	High
CH Idle State	Reset

6.12 USART1

Mode: Asynchronous

6.12.1 Parameter Setting

Basic Parameters:

Baud Rate(1831-7500000)	115200
Data bit num	8 Bits (including Parity)
Parity selection	None
STOP bit num	1

Advanced Parameters:

Data Direction	Receive and Transmit

6.13 USBFS

Device(FS): Enable

6.14 WDT

Activated: Enable

6.14.1 Parameter Setting

Clocking:

WDT counter clock prescaler	4
WDT down-counter reload value(0x0-0xFFF)	0xFFF

6.15 WWDT

Activated: Enable

6.15.1 Parameter Setting

Clocking:

WWDT counter clock prescaler	4096
WWDT window value(0x40-0x7F)	0x40
WWDT downcounter value(0x40-0x7F)	0x40

7 System Configuration

7.1 GPIO Configuration

IP	Pin Name	Signal	Output level	GPIO type	Pull type	GPIO mode	Driver capability	Label
DEBUG	PA13	DEBUG_JTMS_SWDIO	n/a	n/a	n/a	n/a	n/a	
	PA14	DEBUG_JTCK_SWCLK	n/a	n/a	n/a	n/a	n/a	
	PA15	DEBUG_JTDI	n/a	n/a	n/a	n/a	n/a	
	PB3	DEBUG_JTDO	n/a	n/a	n/a	n/a	n/a	
	PB4	DEBUG_NJTRST	n/a	n/a	n/a	n/a	n/a	
EMAC	PC1	EMAC_MDC	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PA1	EMAC_RMII_REF_CLK	n/a	n/a	Pull-none	Input mode	n/a	
	PA2	EMAC_MDIO	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PA7	EMAC_RMII_CRS_DV	n/a	n/a	Pull-none	Input mode	n/a	
	PC4	EMAC_RMII_RXD0	n/a	n/a	Pull-none	Input mode	n/a	
	PC5	EMAC_RMII_RXD1	n/a	n/a	Pull-none	Input mode	n/a	
	PB11	EMAC_RMII_TX_EN	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PB12	EMAC_RMII_TXD0	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PB13	EMAC_RMII_TXD1	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
I2C1	PB6	I2C1_SCL	n/a	Open Drain	Pull-none	Mux function mode	Moderate	
	PB7	I2C1_SDA	n/a	Open Drain	Pull-none	Mux function mode	Moderate	
I2C3	PC9	I2C3_SDA	n/a	Open Drain	Pull-none	Mux function mode	Moderate	
	PA8	I2C3_SCL	n/a	Open Drain	Pull-none	Mux function mode	Moderate	

I2S4	PE2	I2S4_CK	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PE4	I2S4_WS	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PE6	I2S4_SD	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
PWC	PA0	WKUP	n/a	n/a	n/a	n/a	n/a	
RTC	PC13	RTC_TAMPER	n/a	n/a	n/a	n/a	n/a	
SDIO1	PC8	SDIO1_D0	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PC12	SDIO1_CK	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PD2	SDIO1_CMD	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
SPI1	PA5	SPI1_SCK	n/a	n/a	Pull-none	Input mode	n/a	
	PA6	SPI1_MISO	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
TMR1	PE9	TMR1_CH1	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
USART1	PA9	USART1_TX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PA10	USART1_RX	n/a	n/a	Pull-none	Input mode	n/a	
USBFS	PA11	USBFS_D-	n/a	n/a	n/a	n/a	n/a	
	PA12	USBFS_D+	n/a	n/a	n/a	n/a	n/a	

7.2 DMA Configuration

Nothing configuration in DMA Service.

7.3 NVIC Configuration

NVIC Interrupt Table	Enabled	Preemption Priority	Sub Priority
Reset_IRQ	true	0	0
NonMaskableInt_IRQ	true	0	0
HardFault_IRQ	true	0	0
MemoryManagement_IRQ	true	0	0
BusFault_IRQ	true	0	0
UsageFault_IRQ	true	0	0
SVCall_IRQ	true	0	0
DebugMonitor_IRQ	true	0	0
PendSV_IRQ	true	0	0
SysTick_IRQ	Unused		
WWDT_IRQ	Unused		
PVM_IRQ	Unused		
TAMPER_IRQ	Unused		
RTC_IRQ	Unused		
FLASH_IRQ	Unused		
CRM_IRQ	Unused		
EXINT0_IRQ	Unused		
EXINT1_IRQ	Unused		
EXINT2_IRQ	Unused		
EXINT3_IRQ	Unused		
EXINT4_IRQ	Unused		
DMA1_Channel1_IRQ	Unused		
DMA1_Channel2_IRQ	Unused		
DMA1_Channel3_IRQ	Unused		
DMA1_Channel4_IRQ	Unused		
DMA1_Channel5_IRQ	Unused		
DMA1_Channel6_IRQ	Unused		
DMA1_Channel7_IRQ	Unused		
ADC1_2_IRQ	Unused		
USBFS_H_CAN1_TX_IRQ	Unused		
USBFS_L_CAN1_RX0_IRQ	Unused		
CAN1_RX1_IRQ	Unused		
CAN1_SE_IRQ	Unused		
EXINT9_5_IRQ	Unused		

TMR1_BRK_TMR9_IRQ	Unused
TMR1_OVF_TMR10_IRQ	Unused
TMR1_TRG_HALL_TMR11_IRQ	Unused
TMR1_CH_IRQ	Unused
TMR2_GLOBAL_IRQ	Unused
TMR3_GLOBAL_IRQ	Unused
TMR4_GLOBAL_IRQ	Unused
I2C1_EVT_IRQ	Unused
I2C1_ERR_IRQ	Unused
I2C2_EVT_IRQ	Unused
I2C2_ERR_IRQ	Unused
SPI1_IRQ	Unused
SPI2_I2S2EXT_IRQ	Unused
USART1_IRQ	Unused
USART2_IRQ	Unused
USART3_IRQ	Unused
EXINT15_10_IRQ	Unused
RTCAlarm_IRQ	Unused
USBFSWakeUp_IRQ	Unused
TMR8_BRK_TMR12_IRQ	Unused
TMR8_OVF_TMR13_IRQ	Unused
TMR8_TRG_HALL_TMR14_IRQ	Unused
TMR8_CH_IRQ	Unused
ADC3_IRQ	Unused
XMC_IRQ	Unused
SDIO1_IRQ	Unused
TMR5_GLOBAL_IRQ	Unused
SPI3_I2S3EXT_IRQ	Unused
UART4_IRQ	Unused
UART5_IRQ	Unused
TMR6_GLOBAL_IRQ	Unused
TMR7_GLOBAL_IRQ	Unused
DMA2_Channel1_IRQ	Unused
DMA2_Channel2_IRQ	Unused
DMA2_Channel3_IRQ	Unused
DMA2_Channel4_5_IRQ	Unused
SDIO2_IRQ	Unused

I2C3_EVT_IRQ	Unused
I2C3_ERR_IRQ	Unused
SPI4_IRQ	Unused
CAN2_TX_IRQ	Unused
CAN2_RX0_IRQ	Unused
CAN2_RX1_IRQ	Unused
CAN2_SE_IRQ	Unused
ACC_IRQ	Unused
USBFS_MAPH_IRQ	Unused
USBFS_MAPL_IRQ	Unused
DMA2_Channel6_7_IRQ	Unused
USART6_IRQ	Unused
UART7_IRQ	Unused
UART8_IRQ	Unused
EMAC_IRQ	Unused
EMAC_WKUP_IRQ	Unused

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