

1 Overview

1.1 Project

Project Name	AT32F423VCT7_WorkBench
Generated with	AT32 WorkBench V1.0.3
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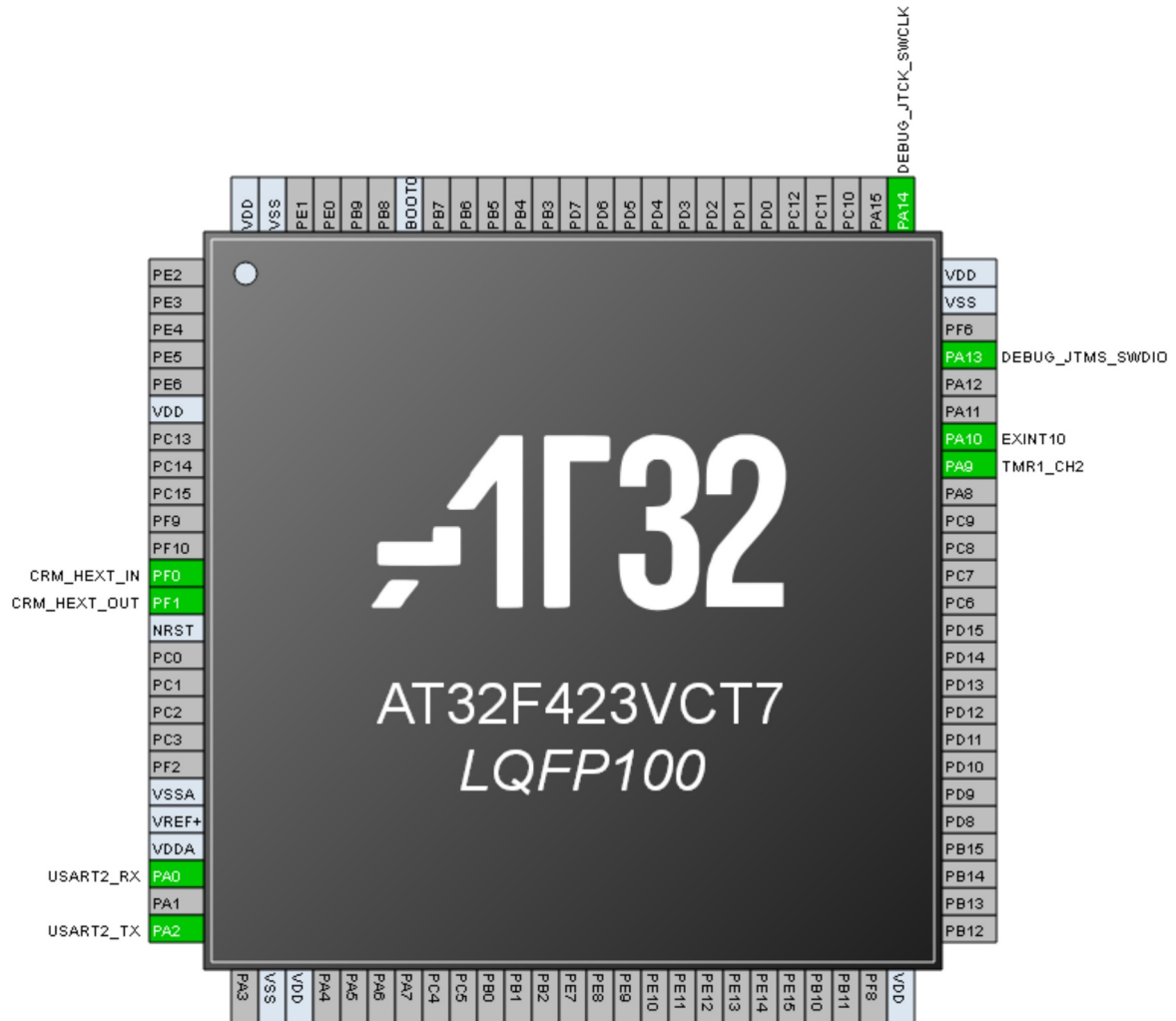
1.2 MCU Information

MCU Series	AT32F423
MCU Name	AT32F423VCT7
MCU Package	LQFP100
MCU Pin number	100
Flash	256KB
SRAM	48KB

1.3 Cores Information

Cores	ARM Cortex-M4
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2 Pinout Configuration



3 Pins Configuration

Pin Number	Pin Name	Pin Type	GPIO Structure	Signal Name	Label
6	VDD	S	-	-	
12	PF0	I/O	TC	CRM_HEXT_IN	
13	PF1	I/O	TC	CRM_HEXT_OUT	
14	NRST	I/O	R	-	
20	VSSA	S	-	-	
21	VREF+	S	-	-	
22	VDDA	S	-	-	
23	PA0	I/O	FTa	USART2_RX	
25	PA2	I/O	FTa	USART2_TX	
27	VSS	S	-	-	
28	VDD	S	-	-	
50	VDD	S	-	-	
68	PA9	I/O	FT	TMR1_CH2	
69	PA10	I/O	FT	EXINT10	
72	PA13	I/O	FT	DEBUG_JTMS_SWDIO	
74	VSS	S	-	-	
75	VDD	S	-	-	
76	PA14	I/O	FT	DEBUG_JTCK_SWCLK	
94	BOOT0	I	B	-	
99	VSS	S	-	-	
100	VDD	S	-	-	

(1) I = input, O = output, S = supply.

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog function, FTf = 5 V-tolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull - up resistor, B = dedicated BOOT0 pin with embedded weak pull - down resistor. Of those, FTa pin has 5 V - tolerant characteristics when configured as input floating, input pull - up, or input pull - down mode. However, it cannot be 5 V - tolerant when analog mode. In this case, its input level should not be higher than $VDD + 0.3V$.

(3) Function availability depend on the selected product part number. Any of GPIOs has EVENTOUT feature.

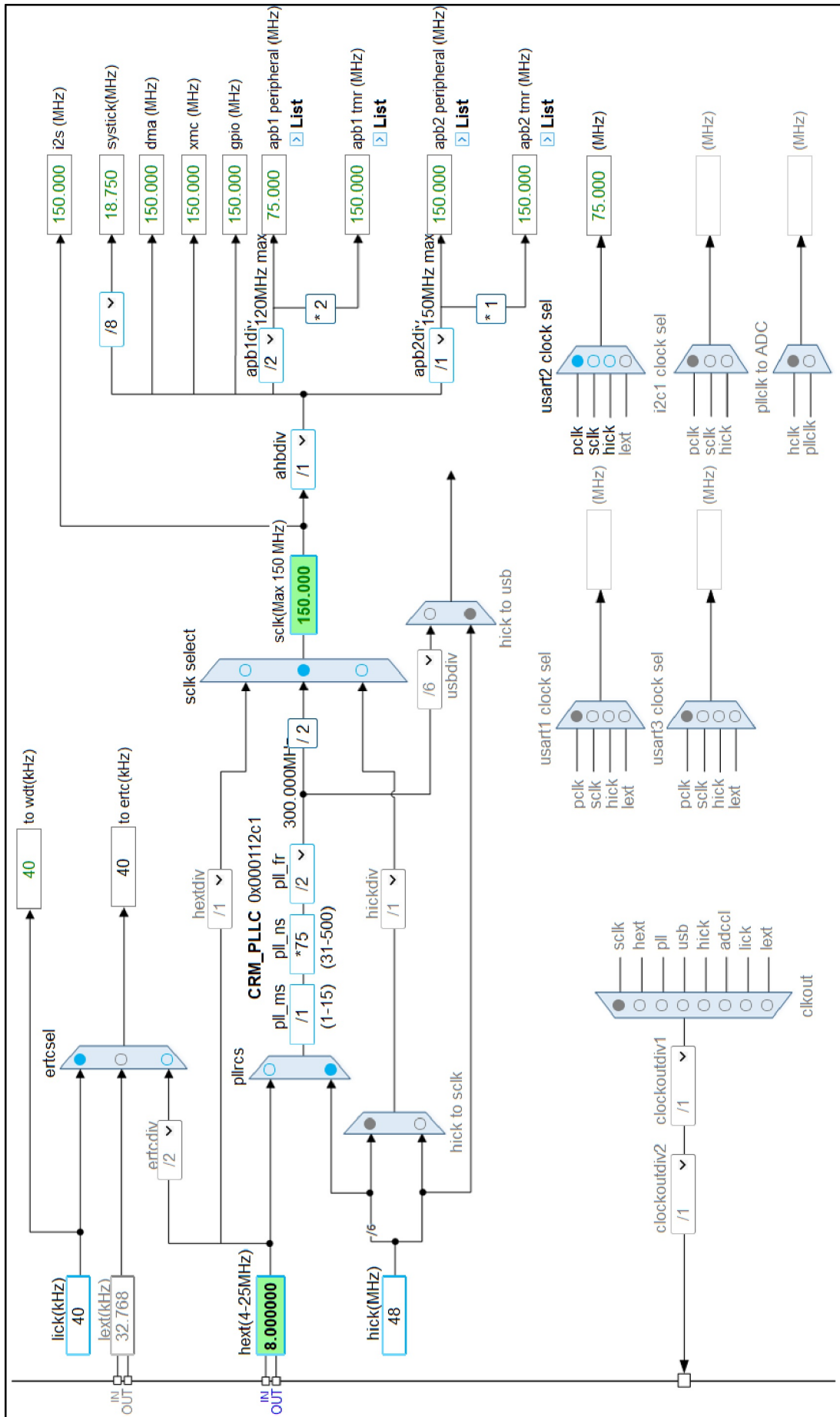
(4) PC13, PC14, and PC15 are supplied through power switch. Since the switch only drives a limited amount of current (3mA), the use of GPIOs PC13 to PC15 in output mode is limited not to be used as a current

source(e.g.to drive an LED).

(5) There are limitations to the use of PC13 and its additional functions. See AT32F423 Errata sheet for details.

(6) PA0, PA1, PC0, PC1, PC2 and PC3 represent fast ADC channel, others slow ADC channels.

4 Clock Tree Configuration



5 Software Project

5.1 Project Settings

Name	Value
Project Name	AT32F423VCT7_WorkBench
Project Folder	C:/Users/ashirov/Downloads/at_sonar_testing
Toolchain/IDE	AT32_IDE
Firmware Package Name and Version	AT32F423_Firmware_Library_EN_V2.0.2(1).zip
Minimum Heap Size	0x200
Minimum Stack Size	0x400

6 Peripherals and Middlewares Configuration

6.1 CRM

High speed external crystal (HEXT): Crystal/Ceramic Resonator

6.2 DEBUG

Debug interface: SWD

6.3 EXINT

EXINT10: Enable

6.3.1 Parameter Setting

EXINT10:

Interrupt/Event	Interrupt
Trigger Polarity	Rising/Falling Edge

6.4 TMR1

Activated: Enable

Channel2 mode: Output_CH2

6.4.1 Parameter Setting

Counter Settings:

Divider value (16 bits value)(0-65535)	1499
Counter Direction	Up
Period Value (16 bits value)(0-65535)	10000
Clock divider	No Divider
Repetition of period value (16 bits value)(0-65535)	0
Period buffer enable	Disable
Overflow Event	From counter/ovfswtr/sub-timer

Primary mode settings:

Synchronize with sub-timer	Disable
Primary TMR output selection	Reset

Break and Dead-time settings:

Break State	Disable
Brake Input Validity	Low
Automatic Output State	Disable

Frozen channel status when holistic output enable	Disable
Frozen channel status when holistic output disable	Disable
Write Protected Configuration	Off

Output Channel 2:

Mode	PWM mode A
Channel data (16 bits value)(0-65535)	10
Channel output buffer	Disable
Immediately Mode	Disable
CH Polarity	High
CH Idle State	Reset

6.5 TMR2

Activated: Enable**Channel1 mode: Output without pin**

6.5.1 Parameter Setting

Counter Settings:

Divider value (16 bits value)(0-65535)	149
Counter Direction	Up
Period Value (16 bits value)(0-65535)	65535
Clock divider	No Divider
Period buffer enable	Disable
Overflow Event	From counter/ovfswtr/sub-timer

Primary mode settings:

Synchronize with sub-timer	Disable
Primary TMR output selection	Reset

Output No Output Channel 1:

Mode	Disconnected
Channel data (16 bits value)(0-65535)	0
Channel output buffer	Disable
CH Polarity	High

6.6 USART2

Mode: Asynchronous

6.6.1 Parameter Setting

Basic Parameters:

Baud Rate(1144-4687500)	115200
Data bit num	8 Bits (including Parity)
Parity selection	None

STOP bit num 1

Advanced Parameters:

Data Direction Receive and Transmit

Advanced Features:

TX polarity reverse Disable

RX polarity reverse Disable

TX and RX Pins Swapping Disable

DT register polarity reverse Disable

MSB transmit first Disable

7 System Configuration

7.1 GPIO Configuration

IP	Pin Name	Signal	Output level	GPIO type	Pull type	GPIO mode	Driver capability	Label
CRM	PF0	CRM_HEXT_IN	n/a	n/a	n/a	n/a	n/a	
	PF1	CRM_HEXT_OUT	n/a	n/a	n/a	n/a	n/a	
DEBUG	PA13	DEBUG_JTMS_SWDIO	n/a	n/a	n/a	n/a	n/a	
	PA14	DEBUG_JTCK_SWCLK	n/a	n/a	n/a	n/a	n/a	
EXINT	PA10	EXINT10	n/a	n/a	Pull-none	Input mode	n/a	
TMR1	PA9	TMR1_CH2	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
USART2	PA0	USART2_RX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	
	PA2	USART2_TX	n/a	Push Pull	Pull-none	Mux function mode	Moderate	

7.2 DMA Configuration

Nothing configuration in DMA Service.

7.3 NVIC Configuration

NVIC Interrupt Table	Enabled	Preemption Priority	Sub Priority
Reset_IRQ	true	0	0
NonMaskableInt_IRQ	true	0	0
HardFault_IRQ	true	0	0
MemoryManagement_IRQ	true	0	0
BusFault_IRQ	true	0	0
UsageFault_IRQ	true	0	0
SVCALL_IRQ	true	0	0
DebugMonitor_IRQ	true	0	0
PendSV_IRQ	true	0	0
SysTick_IRQ		Unused	
WWDT_IRQ		Unused	
PVM_IRQ		Unused	
TAMP_STAMP_IRQ		Unused	
ERTC_WKUP_IRQ		Unused	
FLASH_IRQ		Unused	
CRM_IRQ		Unused	
EXINT0_IRQ		Unused	
EXINT1_IRQ		Unused	
EXINT2_IRQ		Unused	
EXINT3_IRQ		Unused	
EXINT4_IRQ		Unused	
DMA1_Channel1_IRQ		Unused	
DMA1_Channel2_IRQ		Unused	
DMA1_Channel3_IRQ		Unused	
DMA1_Channel4_IRQ		Unused	
DMA1_Channel5_IRQ		Unused	
DMA1_Channel6_IRQ		Unused	
DMA1_Channel7_IRQ		Unused	
ADC1_IRQ		Unused	
CAN1_TX_IRQ		Unused	
CAN1_RX0_IRQ		Unused	
CAN1_RX1_IRQ		Unused	
CAN1_SE_IRQ		Unused	
EXINT9_5_IRQ		Unused	

TMR1_BRK_TMR9_IRQ	Unused
TMR1_OVF_TMR10_IRQ	Unused
TMR1_TRG_HALL_TMR11_IRQ	Unused
TMR1_CH_IRQ	Unused
TMR2_GLOBAL_IRQ	Unused
TMR3_GLOBAL_IRQ	Unused
TMR4_GLOBAL_IRQ	Unused
I2C1_EVT_IRQ	Unused
I2C1_ERR_IRQ	Unused
I2C2_EVT_IRQ	Unused
I2C2_ERR_IRQ	Unused
SPI1_IRQ	Unused
SPI2_IRQ	Unused
USART1_IRQ	Unused
USART2_IRQ	Unused
USART3_IRQ	Unused
EXINT15_10_IRQ	Unused
ERTCAIarm_IRQ	Unused
OTGFS1_WKUP_IRQ	Unused
TMR12_GLOBAL_IRQ	Unused
TMR13_GLOBAL_IRQ	Unused
TMR14_GLOBAL_IRQ	Unused
SPI3_IRQ	Unused
USART4_IRQ	Unused
USART5_IRQ	Unused
TMR6_DAC_GLOBAL_IRQ	Unused
TMR7_GLOBAL_IRQ	Unused
DMA2_Channel1_IRQ	Unused
DMA2_Channel2_IRQ	Unused
DMA2_Channel3_IRQ	Unused
DMA2_Channel4_IRQ	Unused
DMA2_Channel5_IRQ	Unused
CAN2_TX_IRQ	Unused
CAN2_RX0_IRQ	Unused
CAN2_RX1_IRQ	Unused
CAN2_SE_IRQ	Unused
OTGFS1_IRQ	Unused

DMA2_Channel6_IRQ	Unused
DMA2_Channel7_IRQ	Unused
USART6_IRQ	Unused
I2C3_EVT_IRQ	Unused
I2C3_ERR_IRQ	Unused
FPU_IRQ	Unused
USART7_IRQ	Unused
USART8_IRQ	Unused
DMAMUX_IRQ	Unused
ACC_IRQ	Unused

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